6.5. Exact MOS analysis

6.5.1. Introduction

An exact analytic solution can be obtained for the MOS capacitance as long as surface electron concentration is not degenerate. Poisson's equation can then be solved yielding first the electric field as a function of the potential in the semiconductor. A solution for the electric field and/or the potential as a function of the position cannot be obtained analytically. This requires a numeric integration. Combining the electrical field and the surface potential yields the gate voltage, since the field in the semiconductor and that in the oxide are related by their respective dielectric constants. The same approach also yields a good approximation for the charge in the depletion layer, the inversion layer or the accumulation layer. The derivative of the charge with the applied voltage equals the capacitance of the MOS structure. The calculation of the low frequency or quasi-static capacitance is relative straight forward, while the calculation of the high-frequency capacitance requires an additional numeric integration. A detailed derivation of the items mentioned above as well as the deep depletion capacitance and an approximate expression for the high-frequency capacitance can be found in the full derivation.

6.5.2. Electric field versus surface potential

The solution for the electric field is obtained by solving Poisson's equation while including the charge due to electrons, holes and the ionized donors and acceptors. This solution provides the relation between the electric field at the surface of the semiconductor and the surface potential. The absolute value of the field is shown in the figure below. This figure was obtained for a substrate with an acceptor concentration, $N_a = 10^{17}$ cm^{-3}, and an oxide thickness, $t_{ox} = 20$ nm.

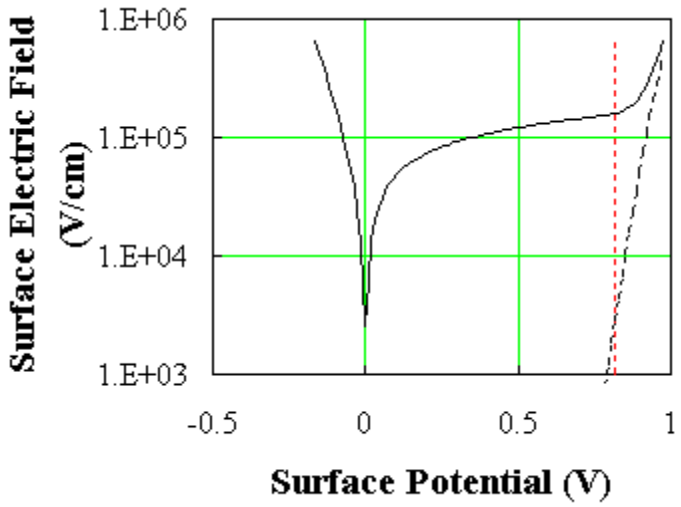

Figure 6.5.1 Electric field at the surface of the semiconductor as a function of the potential across the semiconductor. Shown is the electric field (solid line) and the field due to the inversion layer charge only (black dotted line) The red vertical line indicates the threshold voltage. $N_a = 10^{17}$ cm^{-3} and $t_{ox} = 20$ nm.

When applying a positive potential (which can be done by applying a positive gate voltage) the surface of the silicon is first depleted. This causes an electric field, which varies as the square

root of the surface potential. At higher positive potential the surface inverts which results in a sharp rise of the electric field since the inversion layer charge increases exponentially with the surface potential. The vertical dotted line on the figure indicates the threshold voltage or the onset of strong inversion. The other dotted line represents the fraction of the surface field, which is due to the electrons in the inversion layer. It is calculated from the ratio of the inversion layer charge and the dielectric constant of the semiconductor.

When applying a negative surface potential, the holes accumulate at the surface, yielding an exponential rise of the electric field with decreasing potential.

An MOS structure with a n-type substrate can also be analyzed by entering a negative doping density.

6.5.3. Charge in the inversion layer

The total charge in the inversion layer can also be calculated with this method. It is obtained by subtracting the charge in the depletion layer from the total charge for the same surface potential. The details can be found in the full derivation. The gate voltage is obtained by adding the flat band voltage, the surface potential and the voltage across the oxide. The resulting charge density is plotted versus the gate voltage in the figure below. This figure was calculated for an oxide thickness of 20 nm. The doping density is also 10^{17} cm^{-3} as before.

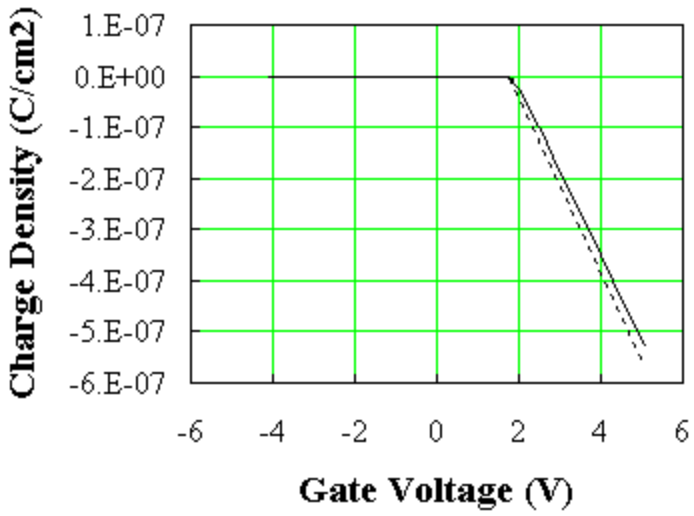

Figure 6.5.2 Charge density due to electrons in the inversion layer of an MOS capacitor. Compared are the analytic solution (solid line) and our basic assumption (dotted line). $N_a = 10^{17}$ cm^{-3} and $t_{ox} = 20$ nm.

The dotted line on the figure represents the standard approximation for the inversion layer charge: it implies that the charge is simply proportional to the gate oxide capacitance and the gate voltage minus the threshold voltage. For voltages below the threshold voltage, there is no inversion layer and therefore no inversion layer charge. While not exact, the standard approximation is very good.

6.5.4. Low frequency capacitance

The low frequency or quasi-static capacitance can be obtained by taking the derivative of the charge in the semiconductor with respect to the potential across the semiconductor. Since this derivative represents the change between two thermal equilibrium situations, this capacitance is also to be measured while maintaining equilibrium conditions at all times. The low frequency or quasi-static measurement is typically obtained by measuring the current with a sensitive electrometer while varying the applied gate voltage.

The expected behavior of such measurement is shown in the figure below: The capacitance is close to the oxide capacitance except for a gate voltage between the flat band voltage and the threshold voltage, as charge is then added deeper into the semiconductor at the edge of the depletion layer, rather than at the oxide-silicon interface. This results in the characteristic dip in the capacitance curve.

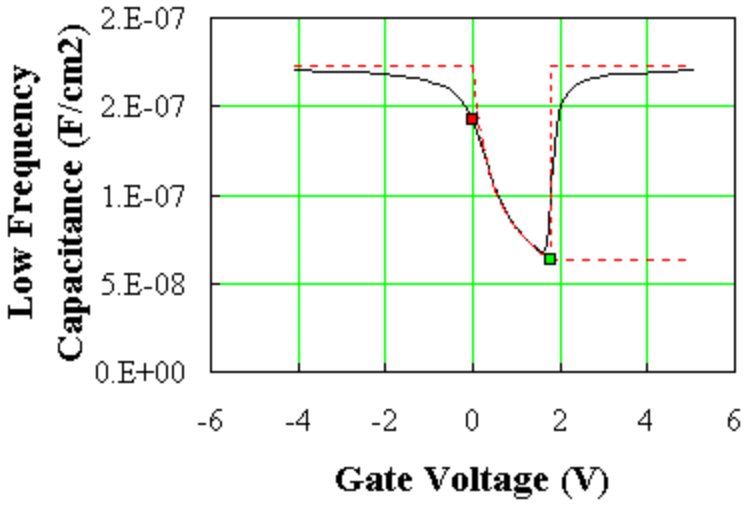

Figure 6.5.3 Low frequency capacitance of an MOS capacitor. Shown is the exact solution for the low frequency capacitance (solid line) and the low and high frequency capacitance obtained with the simple model (dotted lines). The red square indicates the flatband voltage and capacitance, while the green square indicates the threshold voltage and capacitance. $N_a = 10^{17}$ cm^{-3} and $t_{ox} = 20$ nm.

This figure was calculated using an oxide thickness of 20 nm and an acceptor concentration of 10^{17} cm^{-3}. The dotted lines indicate the high- and low-frequency capacitance as obtained using the full depletion approximation. It is clear from the figure that the approximation is rather crude when it comes to describing the full behavior, but it is sufficient to extract the oxide thickness and substrate doping concentration from a measured curve.

6.5.5. Derivation of the exact solution

We now derive the exact solution of the MOS capacitor. Whereas most of the derivation is applicable for *n*-type and *p*-type substrates, the equations are written in a form, which is more convenient for *p*-type substrates, but can be rewritten for n-type substrates.

The total charge density, r, in the semiconductor is given by:

$$r = q(p + N_d^+ - n - N_a^-) \tag{6.5.1}$$

Under thermal equilibrium, the hole and electron densities, p and n, can be expressed as a function of the potential, f, and a reference potential, f_F.

$$p = n_i \exp(\frac{f_F - f(x)}{V_t}) \tag{6.5.2}$$

$$n = n_i \exp(\frac{f(x) - f_F}{V_t}) \tag{6.5.3}$$

far away from the oxide-semiconductor interface, the charge density is zero and we define the potential, f, to be zero there also, so that

$$N_d^+ - N_a^- = -2n_i \sinh(\frac{f_F}{V_t}) \tag{6.5.4}$$

Poisson's equation then takes the following form:

$$\frac{d^2 f}{dx^2} = \frac{2qn_i}{e_s}\{\sinh(\frac{f - f_F}{V_t}) + \sinh(\frac{f_F}{V_t})\} \tag{6.5.5}$$

multiplying both sides of the equation with 2 df/dx and integrating while replacing $-df/dx$ by the electric field E, one obtains:

$$E(f) = \text{sign}(f)\sqrt{\frac{4qn_i V_t}{e_s}\{\cosh(\frac{f - f_F}{V_t}) + \frac{f}{V_t}\sinh(\frac{f_F}{V_t}) + K\}} \tag{6.5.6}$$

the constant K can be determined from the boundary condition at $x = \infty$ where $f = E = 0$ yielding

$$K = -\cosh(\frac{f_F}{V_t}) \tag{6.5.7}$$

The electric field has the same sign as the potential as described with the sign function.

The relation between the field and the potential at the surface under thermal equilibrium is then:

$$E_{s,eq} = 2\,\mathrm{sign}(f_s)\sqrt{\frac{qn_i V_t}{e_s}\{\cosh(\frac{f_s - f_F}{V_t}) + \frac{f_s}{V_t}\sinh(\frac{f_F}{V_t}) - \cosh(\frac{f_F}{V_t})\}} \tag{6.5.8}$$

The gate voltage can be expressed as a function of the flatband voltage, the voltage across the oxide and the potential across the semiconductor:

$$V_G = V_{FB} + f_s + V_{ox}, \text{ with } V_{ox} = t_{ox}E_{s,eq}(f_s)\frac{e_s}{e_{ox}} \tag{6.5.9}$$

6.5.5.1. Low frequency capacitance

The low frequency capacitance of the MOS structure per unit area can then be calculated from:

$$C_{LF} = \left|\frac{dQ_s}{dV_G}\right| = e_s \frac{dE_{s,eq}}{d(f_s + t_{ox}E_{s,eq}(f_s)\frac{e_s}{e_{ox}})} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{s,LF}}} \tag{6.5.10}$$

where $C_{ox} = e_{ox}/t_{ox}$ and

$$C_{s,LF} = e_s \frac{dE_{s,eq}}{df_s} \tag{6.5.11}$$

$$= e_s\sqrt{\frac{qn_i}{e_s V_t}} \frac{\left|\sinh(\frac{f_s - f_F}{V_t}) + \sinh(\frac{f_F}{V_t})\right|}{\sqrt{\cosh(\frac{f_s - f_F}{V_t}) + \frac{f_s}{V_t}\sinh(\frac{f_F}{V_t}) - \cosh(\frac{f_F}{V_t})}}$$

$$C_{s,LF} = 2\frac{qn_i}{E_{s,eq}}[\sinh(\frac{f_s - f_F}{V_t}) + \sinh(\frac{f_F}{V_t})] \tag{6.5.12}$$

This result is often referred to as the low frequency capacitance of a MOS capacitor since we calculated the change in charge between two equilibrium situations. The result can be interpreted as a series connection of the oxide capacitance and the low frequency capacitance of the semiconductor $C_{s,LF}$. By starting from a series of values for f_s, one can use the above equations to first calculate the electric field, the gate voltage and the capacitance. This enables to plot the low frequency capacitance as a function of the gate voltage as shown in Figure 6.5.4.

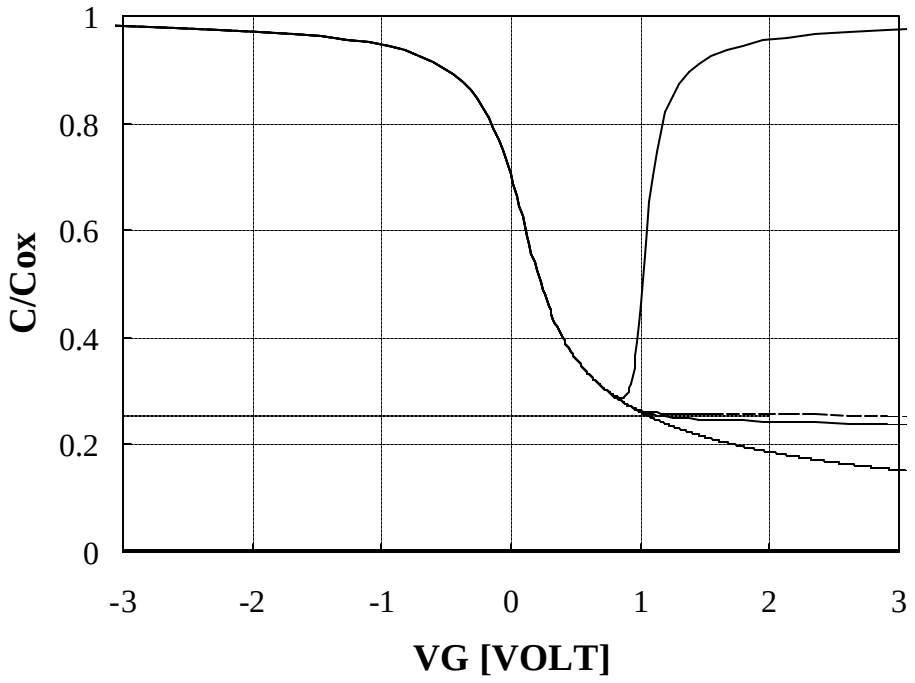

Figure 6.5.4 Capacitance versus voltage for a MOS structure with $N_a = 10^{15}$ cm^{-3} and t_{ox} = 0.1 μm. The curves from top to bottom are: The low frequency capacitance, the approximate high frequency capacitance, the exact high frequency capacitance and the capacitance under deep depletion conditions. The dotted line indicates C_{min}, the capacitance at the onset of strong inversion calculated using the full depletion approximation.

Under flat-band conditions, where $0 = |f_s| < V_t$, the capacitance reduces to

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{e_s}} \tag{6.5.13}$$

where L_D is the extrinsic Debye length in the semiconductor with doping $|N_a - N_d|$:

$$L_D = \sqrt{\frac{e_s V_t}{q|N_a - N_d|}} \tag{6.5.14}$$

6.5.5.2.Deep depletion capacitance

If the gate voltage is changed faster than electrons can be generated at the oxide-semiconductor interface to obtain the equilibrium density, no inversion layer is generated. In this case the gate voltage will cause the depletion layer in the semiconductor to exceed the maximum depletion layer width as defined at the onset of strong inversion. A typical measurement starts from an

equilibrium situation where no inversion layer is present and the gate voltage is swept rapidly while creating a depletion layer in the semiconductor. The capacitance is measured as the change in charge flowing into the structure for a given voltage change. For a *p*-type substrate, this situation can be modeled by eliminating the charge term due to electrons in Poisson's equation:

$$\frac{d^2f}{dx^2} = \frac{qn_i}{e_s}\{2\sinh(\frac{f_F}{V_t}) - \exp(\frac{f_F - f}{V_t})\} \tag{6.5.15}$$

Using the same procedure as above the relation between surface field and surface potential can be found:

$$E_{s,dd} = \text{sign}(f_s)\sqrt{\frac{2qn_iV_t}{e_s}\{2\frac{f_s}{V_t}\sinh(\frac{f_F}{V_t}) + \exp(\frac{f_F}{V_t})(\exp(\frac{-f_s}{V_t}) - 1)\}} \tag{6.5.16}$$

and the capacitance of the semiconductor becomes:

$$C_{s,dd} = \left|\frac{qn_i}{E_{s,dd}}[2\sinh(\frac{f_F}{V_t}) - \exp(\frac{f_F - f_s}{V_t})]\right| \tag{6.5.17}$$

and the corresponding gate voltage is:

$$V_G = V_{FB} + f_s + V_{ox}, \text{ with } V_{ox} = t_{ox}E_{s,dd}(f_s)\frac{e_s}{e_{ox}} \tag{6.5.18}$$

Using a similar procedure as for the low frequency capacitance we can also plot the capacitance under deep depletion conditions.

6.5.5.3.High frequency capacitance

The high frequency capacitance of an MOS capacitor is measured by applying a small ac voltage in addition to the DC gate voltage. The capacitance is defined as the ratio of the out-of-phase component of the ac current divided by the amplitude of the ac voltage times the radial frequency. An approximate expression can be obtained by ignoring the change in charge in the inversion layer yielding the expression for the capacitance under deep depletion conditions. However since the gate voltage is changed slowly while measuring the capacitance versus voltage, the gate voltage is calculated from the surface potential including the charge in the inversion layer under thermal equilibrium. The capacitance is then given by:

$$C_{s,HF} = \left|\frac{qn_i}{E_{s,dd}}[2\sinh(\frac{f_F}{V_t}) - \exp(\frac{f_F - f_s}{V_t})]\right| \tag{6.5.19}$$

with the electric field, $E_{s,dd}$, obtained under deep depletion conditions (6.5.16).

This is the same expression as for the capacitance under deep depletion conditions. However, the corresponding gate voltage is different, namely:

$$V_G = V_{FB} + f_s + V_{ox}, \text{ with } V_{ox} = t_{ox}E_{s,eq}(f_s)\frac{e_s}{e_{ox}} \tag{6.5.20}$$

where the electric field, $E_{s,eq}$, is the thermal equilibrium field

The corresponding capacitance is also included in Figure 6.5.4 together with the expected minimum capacitance based on the full depletion approximation corrected for the thermal voltage:

$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \sqrt{\frac{2\,(2f_F + V_t)}{qN_a e_s}} \tag{6.5.21}$$

It should be stressed that this is only an approximate solution. The redistribution of the inversion layer charge with applied gate voltage is ignored in the approximate solution even though it does affect the depletion layer width and with it the capacitance. This approximation therefore introduces an error which was found to be less than 6% at the onset of strong inversion and which increases almost linearly with increasing surface potential.

The exact expression for the high frequency capacitance[1] used in Figure 6.5.4 is:

$$C_{s,HF,exact} = \frac{qn_i\,sign(f_s)}{E_{s,eq}} \times\left\{\exp(U_F)[1-\exp(-U_s)] + \exp(-U_F)\frac{[\exp(U_s)-1]}{1+\Delta}\right\} \tag{6.5.22}$$

Where Δ for a *p*-type substrate is:

$$\Delta = 0 \text{ for } f_s < 0 \text{ and } f_F > 0 \tag{6.5.23}$$

$$\Delta = \frac{\dfrac{(\exp(U_S) - U_S - 1)}{F(U_S \mid U_F)}}{\displaystyle\int_0^{U_s} \frac{\exp(U_F)(1-\exp(-x))(\exp(-x)-x-1)}{2F^3(x \mid U_F)}\,dx} \text{ for } f_s > 0 \text{ and } f_F > 0 \tag{6.5.24}$$

The expression with $\Delta = 0$ for all possible surface potentials equals the low frequency capacitance. The function *F* is related to the equilibrium electric field by:

$$F(U \mid U_F) = \frac{E_{eq} L_{D,i}}{2\sqrt{2}\,V_t} \tag{6.5.25}$$

and the normalized parameters *U*, U_s and U_F are defined as:

$$U = f/V_t,\ U_s = f_s/V_t, U_F = f_F/V_t \tag{6.5.26}$$

Where the gate voltage is still given by:

---

[1] A derivation of this expression can be found in "MOS (Metal Oxide Semiconductor) Physics and Technology", E. H. Nicollian and J. R. Brews, Wiley and Sons, 1982, p 157.

$$V_G = V_{FB} + f_s + V_{ox}, \text{ with } V_{ox} = t_{ox} E_{s,eq}(f_s) \frac{e_s}{e_{ox}} \tag{6.5.27}$$

and the electric field, $E_{s,eq}$, is the thermal equilibrium field at the surface.

As illustrated with Fig.A6.2, the high frequency capacitance at the onset of strong inversion ($\phi_S=2\phi_F$) and beyond is found to be almost constant. Assuming $\phi_F >> V_t$ one finds

$$C_{s,HF} = \sqrt{\frac{qN_a e_s}{4f_F}}, \text{ for } V_G - V_{FB} > 2f_F + \frac{\sqrt{4qN_a e_s f_F}}{C_{ox}} \tag{6.5.28}$$

this result could also be obtained by calculating the depletion region width in the semiconductor assuming the maximum potential at the surface to be $2f_F$ and using the full depletion approximation. The low frequency capacitance at $f_s = 2f_F$, assuming $f_F >> V_t$ is then:

$$C_{s,LF} = \sqrt{\frac{2qN_a e_s}{f_F}}, \text{ for } V_G - V_{FB} = 2f_F + \frac{\sqrt{4qN_a e_s f_F}}{C_{ox}} \tag{6.5.29}$$

also yielding the following relation between both:

$$C_{s,LF} = \sqrt{8} C_{s,HF}, \text{ for } f_s = 2f_F \tag{6.5.30}$$